PATENT ABSTRACTS OF JAPAN

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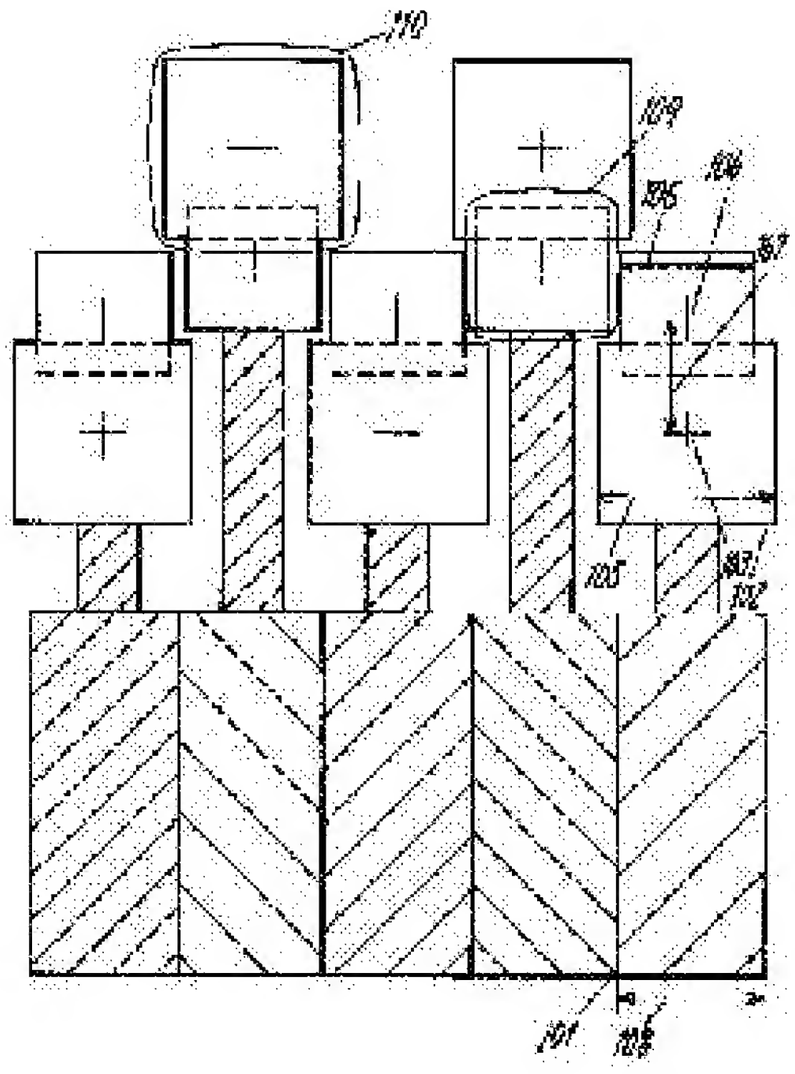
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ASSEMBLING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method which can surely inspect and assemble a semiconductor integrated circuit device, while optimizing the area of an electrode pad, in a semiconductor integrated circuit device in which making into microstructure is made to progress.
SOLUTION: Electrode regions 110 for bonding and bonding regions 109 for inspection are so arranged that the interval between a center 103 of the region 110 and a center 104 of the region 109 becomes greater than or equal to an interval 107. In a semiconductor integrated circuit device having formed electrode pads 102, inspection and bonding are easily and surely enabled by performing inspection and assembling through the use of the centers 103 and 104 of the respective regions.

CLAIMS

[Claim(s)]
[Claim 1]A semiconductor integrated circuit device comprising:
It is an electrode region of the 1st rectangular shape for bonding to each external terminal.
An electrode pad formed by touching and arranging an electrode region of the 2nd rectangular shape for a test.

[Claim 2]To the semiconductor integrated circuit device according to claim 1, contact a test probe pin to the 2nd aforementioned electrode pad, and electrical characteristics inspection of the semiconductor integrated circuit device concerned is conducted, An inspection assembly method of a semiconductor integrated circuit device performing bonding of an external signal line to the 1st aforementioned electrode pad.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001] [Field of the Invention]This invention about realization of the densification of a semiconductor integrated circuit device, and high integration, The pad arrangement for realizing certainly bonding to the electrical characteristics inspection and the package of a semiconductor integrated circuit device which were integrated especially highly, and making area of a semiconductor integrated circuit device as small as possible, The method of performing an electrical property inspection and assembly of the semiconductor integrated circuit device using said pad is provided.
[0002] [Description of the Prior Art]With improvement in the minuteness making art of a semiconductor integrated circuit device in recent years, the inside of a semiconductor integrated circuit device, The directional control of a signal for exchanging an electrical signal with the exterior and the area of the pad cell in which the protection circuit is carried are also reduced substantially, and it is becoming what also has a small pitch of this pad cell.
[0003]Although the minuteness making art in semiconductor manufacturing technology is improving at rapid speed, In the inspection art of applying a pin to an electrode pad and evaluating an electrical property, and the bonding art of making connection between an integrated circuit and a package via an electrode pad, it is becoming difficult to realize minuteness making of the like in semiconductor manufacturing technology.
[0004]Also in [in electrical characteristics inspection, an electrode pad actually needs to secure the field determined from the thickness of the checking pin in test equipment, and the accuracy of a gap of a motion, and] the bonding to a package, An electrode pad needs to secure the field defined with the width of a lead, etc.
[0005]As one of the methods of avoiding, these technical problems in JP,5-206383,A. Apart from an electrode pad, the pad for electrical characteristics inspection is provided, it is arranging this on the dicing line outside the field of an integrated circuit on a semiconductor wafer, the area which is needed in order to perform the inspection of the pad for electrical characteristics inspection is secured, and inspection of IC and facilitating of measurement are attained.
[0006] [Problem(s) to be Solved by the Invention]However, although it makes it possible

to carry out certainly about the inspection of an electrical property in JP,5-206383,A, as conventional technology has described, it is necessary to give fixed width to an electrode pad also for bonding, and this problem cannot be solved.
[0007]At the present, minuteness making also follows a dicing line with improvement in the processing technology of a semiconductor wafer, Even if the width of the pad for electrical characteristics inspection may become large rather than the width of a dicing line and it uses the technique of JP,5-206383,A, it is difficult that it is compatible in facilitating of an inspection of IC and optimization of the area of an integrated circuit.
[0008]In order to perform inspection and bonding, when conducting an electrical property inspection using an electrode pad with a necessary minimum size and trying to perform bonding using the same electrode pad after this, bonding may go wrong. This is the cause with big the probe pin of the inspection tool which guessed when conducting a characteristic inspection leaving probe marks to an electrode pad.
[0009]It is because the rate that the probe marks to the size of an electrode pad occupy becomes large and these probe marks serve as sticking by pressure and hindrance of alloy formation in the case of bonding as the minuteness making of an electrode pad progresses.
[0010] [Means for Solving the Problem]In order to solve the above-mentioned technical problem and to realize an inspection and bonding of a positive electrical property, Area of an electrode pad is expanded, area ratios of probe marks after an inspection are reduced, and how to make bonding possible, or to divide an electrode pad into a portion for performance verification and a portion for bonding, to create it, and to keep probe marks from remaining in a portion of a pad for bonding can be considered.
[0011]In order to realize a positive inspection and bonding in this patent and to attain optimization of area further, an electrode pad, It supposes that a place which carries out a probe, and a place which carries out bonding are changed, and further, in order to attain optimization of area of a semiconductor integrated circuit device, it opts for electrode pad arrangement based on information, including a rule of an inspection, a rule of bonding, and a pad pitch.
[0012] [Embodiment of the Invention]Hereafter, an embodiment of the invention is described using figures.
[0013](A 1st embodiment) A 1st embodiment explains the invention concerning claim 1 using figures.
[0014]Drawing 1 is an example of arrangement of the pad for electrodes designed based on this invention, and this electrode pad. 101 is a pad cell body and a protection circuit and control logic are carried.
[0015]The field 109 is a checking electrode region and the field 110 is an electrode region for bonding. Here, in the field 110, in order to be able to perform bonding certainly, the minimum size is specified, and the width is set to 105 from the physical factor of the accuracy of a bonding device, or a bonding wire. The minimum size is prescribed that the field 109 can ensure an inspection from the accuracy and the checking pin physical characteristic of test equipment, and the width is set to 106.
[0016]The electrode pad 102 is formed by piling up contiguity or a part and arranging said field 109 and the field 110. It is one feature to become a convex shape like the electrode pad 102 in this invention.
[0017]103 is a center position of the pad region 110 for bonding, and 104 has become a

center position of the pad region 109 for performance verification.
[0018]Here, the interval 107 shows the minimum width of the distance of the center 103 of the pad region 110 for bonding, and the center 104 of the checking pad region 109. Even if the probe marks of the pin remain on the pad after placing the pin for probes in the case of a characteristic inspection, if only this interval is maintained, this distance will be the distance for guaranteeing that bonding can be performed certainly, and will turn into the most important distance for this invention. Thus, since that an inspection and bonding are certainly realizable can guarantee even if it piles up and arranges the field 109 and the field 110, while each center 103 and 104 had maintained 107 or more-interval distance by defining the interval 107, The effect of reduction of electrode pads is also expectable.
[0019]Drawing 2 is an example of arrangement of the pad for electrodes designed based on this invention, and this pad for electrodes. Drawing 2 is in the state at the time of the value same in the width 105 of the electrode region for bonding, and the width 106 of a checking electrode region in drawing 1. In such a state, since distinction is lost at the center 203 of the electrode region for bonding, and the center 204 of a checking electrode region, when conducting bonding and an inspection, selection of which to use is attained and an efficient inspection and bonding become possible.
[0020](A 2nd embodiment) A 2nd embodiment explains the invention concerning claim 2 using figures.
[0021]Drawing 3 shows an example of the test method realized by this invention. Here, 301 is a probe pin of verification, contacts this at the center 104 of the electrode region for a test, and performs an electrical property inspection. At this time, by factors, such as an angle of approach over the electrode pad of the accuracy of the distance between pins of a checking probe pin, the accuracy about probe pin movement of test equipment, and a checking probe pin, although the contact place to the electrode pad 102 of the pin 301 shifts from the center position 104, Since the checking electrode region 109 has secured the width 106, it is possible to ensure an inspection.
[0022]Drawing 4 shows an example of the assembly method of a semiconductor circuit device realized by this invention. Here, 401 is a terminal of a package and 402 is a lead which connects a package and a semiconductor integrated circuit device. 403 is probe marks produced at the place where the checking probe pin contacted like drawing 3, and the surface of the pad has got damaged greatly.
[0023]Since it becomes a form where probe marks like [when / same / it performs by the way] 403 are about an inspection and bonding, and also a lead etc. are connected, connection stops thus, succeeding. In this invention, since bonding is performed using the center 103 of the electrode region for bonding, it does not become that a faulty connection happens. Since the electrode 102 has secured the accuracy of a bonding device, and the width 105 of the electrode region for bonding specified from physical conditions like lead line width, the positive assembly has been realized without a faulty connection, a short circuit with the adjoining pad for electrodes, etc. taking place. In this drawing, although the wire-bonding type is explained, this view will become sufficiently effective also to a connection method like a chip-size package or an area pad.
[0024] [Effect of the Invention]In the semiconductor integrated circuit device which minuteness making follows in this invention as explained above, Divide an electrode pad into a checking field and the field for bonding, and it is considered, By realizing the

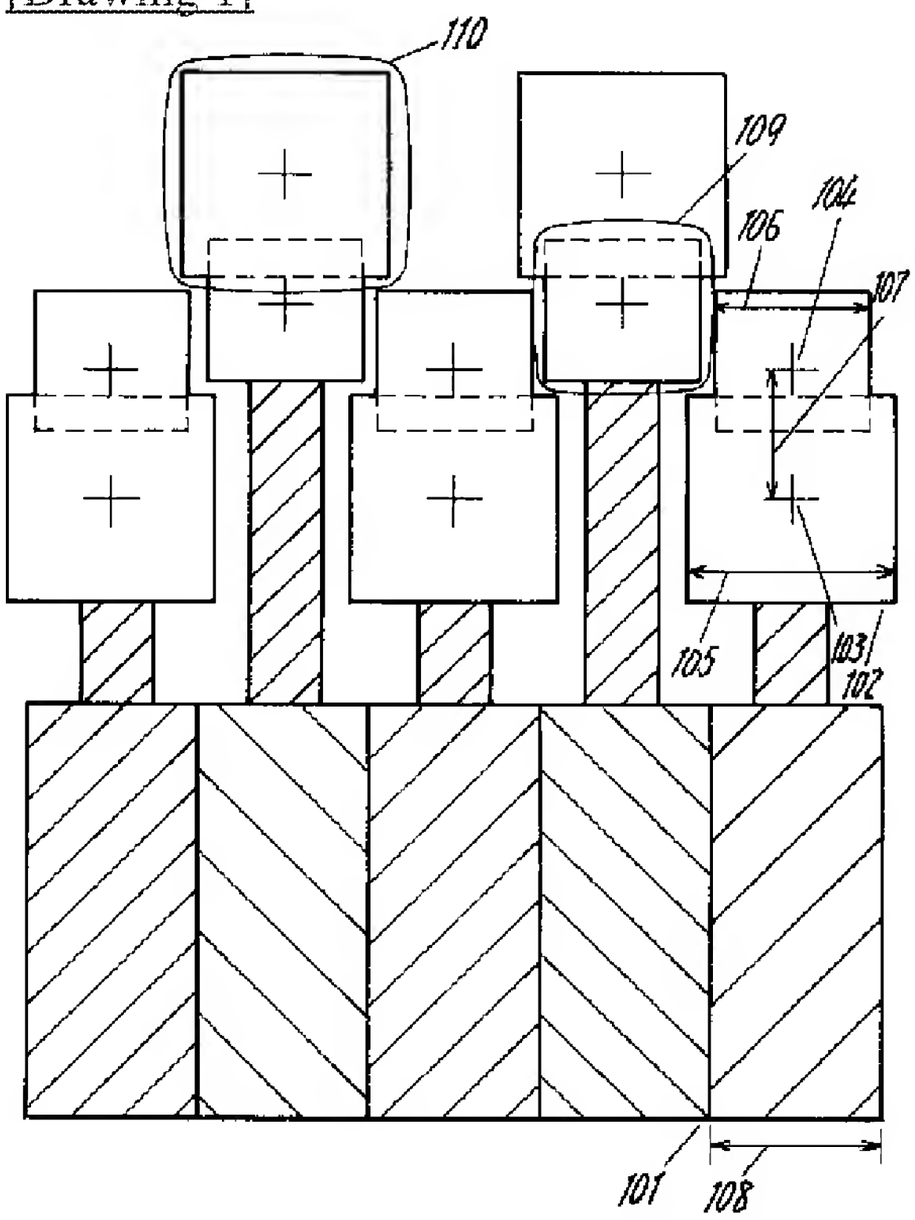
design of this electrode pad so that the width of these fields and the minimum of the interval may be determined based on information, including the accuracy of test equipment and a bonding device, the process tolerance of the pin for probes, etc., and this minimum may be secured. Optimization of area is also realizable while being able to perform an inspection and assembly of a semiconductor integrated circuit device certainly.

DESCRIPTION OF DRAWINGS

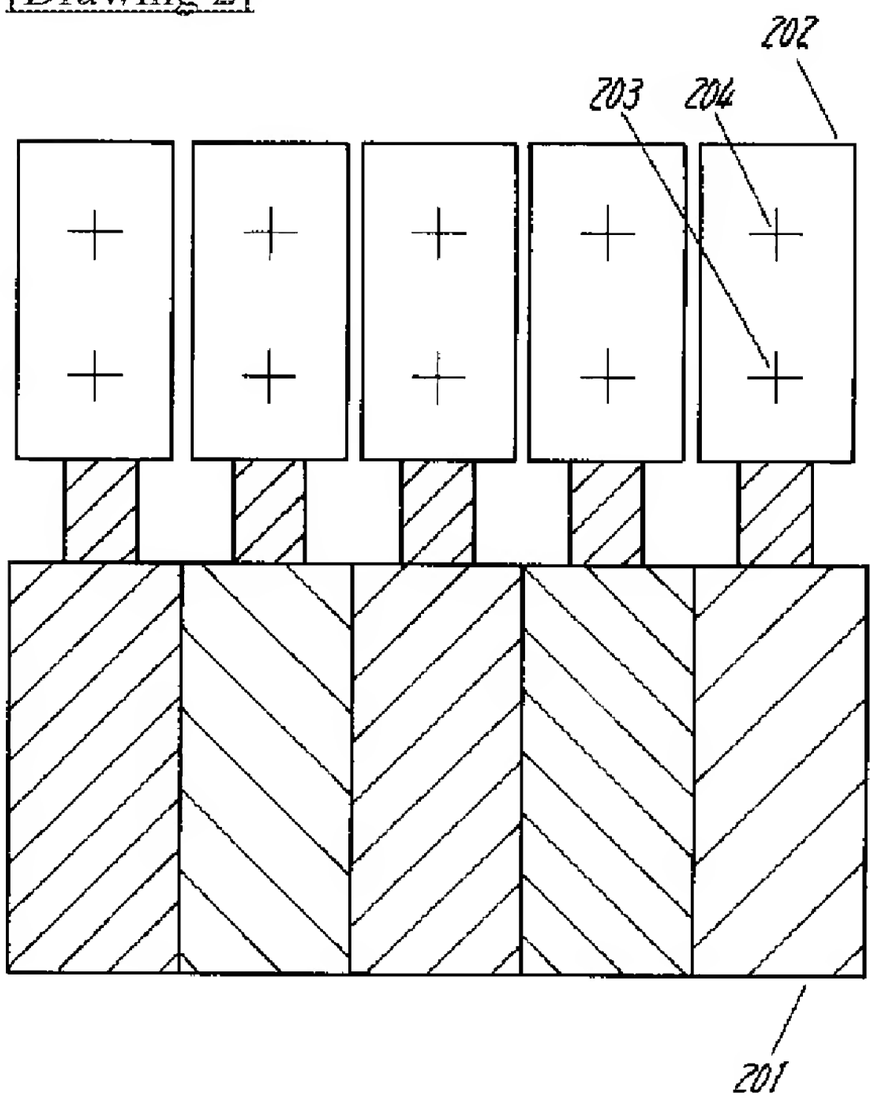
[Brief Description of the Drawings]
[Drawing 1]The figure showing the example of arrangement of the pad for electrodes in a 1st embodiment of this invention
[Drawing 2]The figure showing the example of arrangement of the pad for electrodes in a 1st embodiment of this invention
[Drawing 3]The figure showing an example of the inspection method of the semiconductor integrated circuit device in a 2nd embodiment of this invention
[Drawing 4]The figure showing an example of the assembly method of the semiconductor integrated circuit device in a 2nd embodiment of this invention
[Description of Notations]
101 Pad cell
102 Electrode pad
103 The center position of the electrode region for bonding
104 The center position of a checking electrode region
105 Minimum width of the electrode region for bonding
106 Minimum width of a checking electrode region
107 The minimum interval of the center position of the electrode region for bonding, and the center position of a checking electrode region
108 Pad cell size
109 Checking electrode region
110 The electrode region for bonding

DRAWINGS

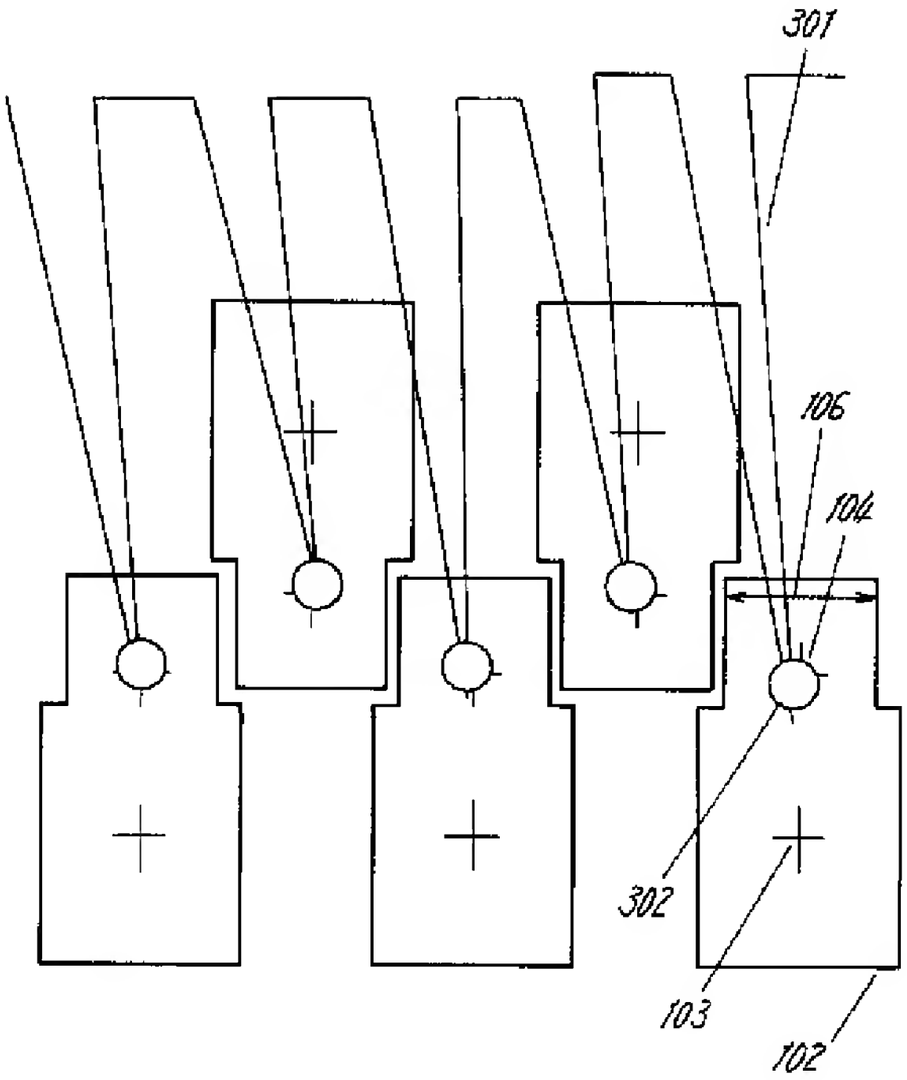
[Drawing 1]



[Drawing 2]



[Drawing 3]



[Drawing 4]